Application of COTS for Early, Low Cost, Avionics System Testbed

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Abstract— The use of flight hardware breadboards to construct an avionics subsystem testbed has been used on Jet Propulsion Laboratory (JPL) projects very successfully. These testbeds provide valuable early integration experience with the flight hardware and software operating together. Commercial off the shelf (COTS) based test systems are integrated with the flight hardware breadboards to create an Avionics testbed platform. The breadboard system has typically consisted of custom-built hardware that was quite expensive and time consuming to build and maintain. With level or decreasing NASA budgets, and faster, better, cheaper project mentality, the flight hardware breadboard has become a target for budget cuts. Since the custom breadboards are not financially feasible, but the need for an early development avionics testbed still apparent, the role of the COTS hardware was expanded to include flight avionics functions. As an added benefit, the COTS hardware is then used as the basis for the flight hardware design.

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1. INTRODUCTION

This paper describes the application of COTS in the Formation Flying Integration Testbed (FIT) that is being constructed at the Jet Propulsion Laboratory for the Space Technology 3 (ST3) project. The ST3 project (launch expected in 2005) is a space based interferometer that is created by two formation flying spacecraft. It is one of the many new spacecraft being developed by JPL that is based on the faster, better, cheaper concept with small budgets and short schedules.

The use of COTS hardware has been increasing steadily at JPL and throughout the aerospace industry. The breadboard avionics described in this paper continues this trend with application of COTS to create a flight avionics breadboard system that can be used to perform high fidelity testing of early versions of the flight software. The flight hardware will be based on the COTS design, which will minimize redesign of the flight software and simplify integration into the testbed.

2. COTS USE IN TEST EQUIPMENT

Avionics subsystem testbeds have been used at JPL extensively to provide an early flight hardware and software integration platform for engineering subsystems and instruments. Testbeds built for JPL spacecraft prior to the nineteen nineties typically relied on expensive custom built hardware that was difficult to maintain and poorly documented. With the advent of a large variety of COTS equipment to support the aerospace and other industries the use of COTS in JPL Testbeds became feasible. This trend has continued throughout the nineties. Vero Modular Eurocard (VME) and more recently Compact Peripheral Computer Interconnect (CPCI) based systems have been relied on heavily to provide embedded real-time computers and interface cards for the complex test and simulation systems used in JPL Testbeds. These COTS systems have proven to be reliable and highly adaptable to solve a wide range of problems encountered by the test and simulation system designers [1].

3. BREADBOARD AVIONICS

In these Testbeds, the COTS based test system would initially be integrated with custom flight breadboards that were typically constructed of large wirewrapped proto-boards or custom printed wiring boards (PWB). During the breadboard test phase, a large number of problems would come to light and major hardware design changes would frequently be required. Once testing of the breadboards was completed and the design was updated to correct any uncovered problems the engineering models would be built and delivered to the Testbed to replace the breadboards and the test cycle would repeat. Typically only a few problems requiring minor hardware design changes would be

uncovered during testing of the engineering models. The design changes would be incorporated into the flight design and flight units would be built and integrated with the COTS test system for flight acceptance testing.

4. ST3 BREADBOARD AVIONICS

The ST3 Breadboard (BB) avionics is an adaptation of a VME based system developed by the Interferometer Technology Program (ITP) at JPL [2] ,[3] and [4]. The COTS components are highlighted in green and makeup a large part of the system. The testbed system is partitioned as test equipment, BB avionics and BB components. There is additional test equipment used for a pseudo star and motion simulator that are not shown since this paper is focusing on COTS used as BB avionics.

A digitized picture of the BB avionics rack in the FIT is shown in figure 1. A close-up view of the rack is shown in figure 2. A high-level block diagram of the avionics interfaced to the test equipment and to the BB components is shown in figure 3.

The BB avionics can be functionally partitioned as follows:

Real-time Computer Subsystem

Optical Delay Line Control

Siderostat Control

CCD Camera Interface

APD Interface

Metrology Interface

Each of these functions will be described below in more detail.

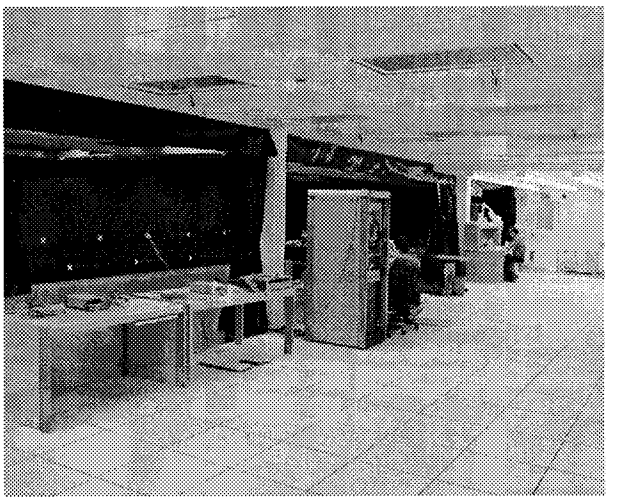

Figure 1 Formation Flying Testbed (FIT) Photo

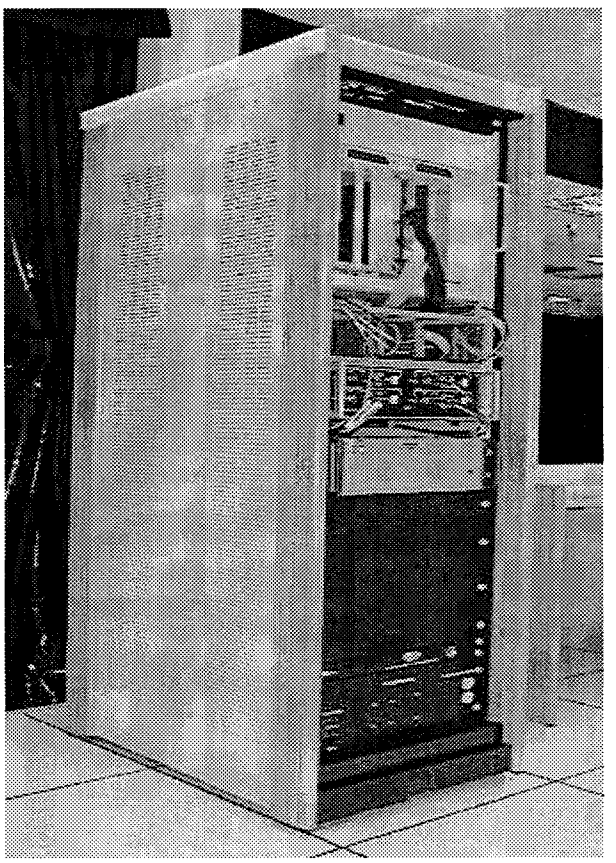

Figure 2 BB Avionics Rack Photo

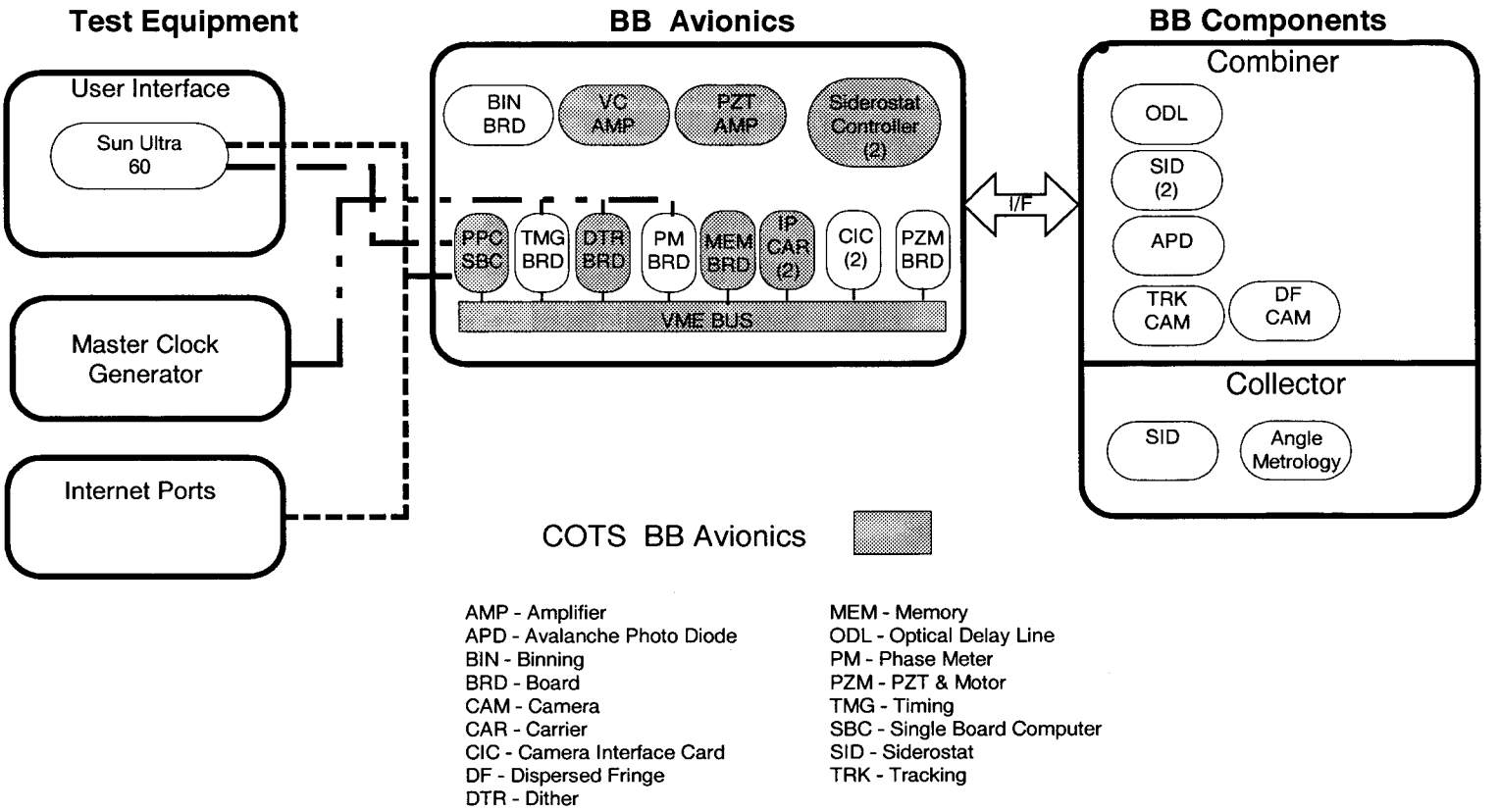

Figure 3 ST3 Testbed High Level Block Diagram

Real-time Computer BB avionics consists of the following components (See Figure 4):

COTS 21 slot, 1000 Watt, VME 64X cage

COTS 300MHZ, Power PC 604 based VME single board computer with 32MB RAM

COTS 16MB VME memory board

Custom VME timing board

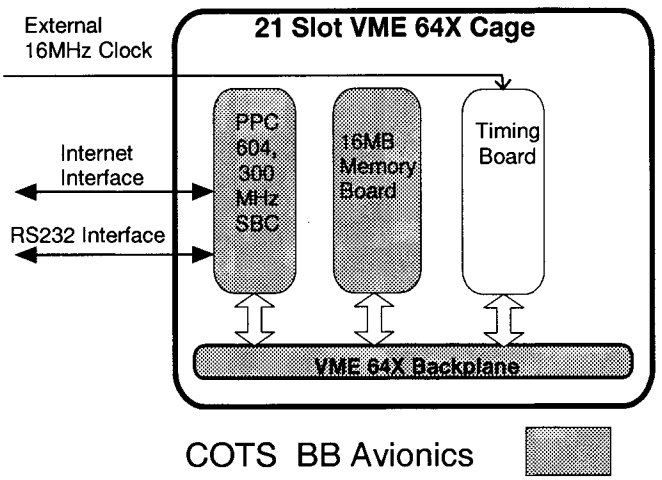

Figure 4 Real-Time Computer Block Diagram

The VME cage has a VME 64X compatible backplane with 6U-form factor, which the VME BB avionics boards plug into. The cage has a 1000W power supply with 3.3V, 5V, and +/-12V voltages. The cage also accommodates mounting VME transition module on the rear panel. The engineering model and flight version avionics boards will be tested in the BB cage. For the flight system, the VME cage

will be replaced with a unit capable of meeting flight environmental and power requirements.

The SBC is an embedded PPC 604 based single board computer running a real-time operating system and executes the flight instrument control software. It has 10/100BaseT Internet interface and RS232 interface for program loading, control, telemetry, and debugging from the test equipment workstation. For flight the SBC will be replaced with a space qualified PPC based SBC that will use the same operating system and be able to execute the flight instrument control software with minimal rewrites.

The 16MB memory card is used for global data storage in multiprocessor application and was not strictly required in this application. It was maintained for software compatibility with other projects. For the flight system RAM on the SBC will most likely be used.

The Timing Card is the master time synchronizer for the system. It provides programmable, periodic VME interrupts that can be used to trigger program execution. In addition, it has external clock and sync inputs and can generate programmable timing outputs. The external clock feature is used to ensure synchronization with the master clock. This is required to achieve accurate metrology data using the phase meter that is also synced to the master clock. The timing card for the flight system will be based on this design and modified to meet flight requirements.

The Optical Delay Line BB avionics consists of the following components (See Figure 5):

COTS 16Bit, 3-channel, analog output IP module

COTS Current Mode Power Supply

COTS DC Motor Controller

COTS High Voltage PZT Amp

COTS 16Bit, 8-channel waveform generator board

Custom PZT/Motor board

The analog output IP module provides +/-10V control signals to the current mode power supply and the DC motor controller. For flight a space-qualified version of the IP module will be developed.

The DC motor controller drives a DC motor that provides the coarse stage control of the ODL. The controller will be replaced in the flight configuration by a custom space qualified design.

The current mode power supply is used to drive the ODL voice coil actuator, which will be replaced by a custom JPL designed current mode power supply that will be powered from the spacecraft 28V power.

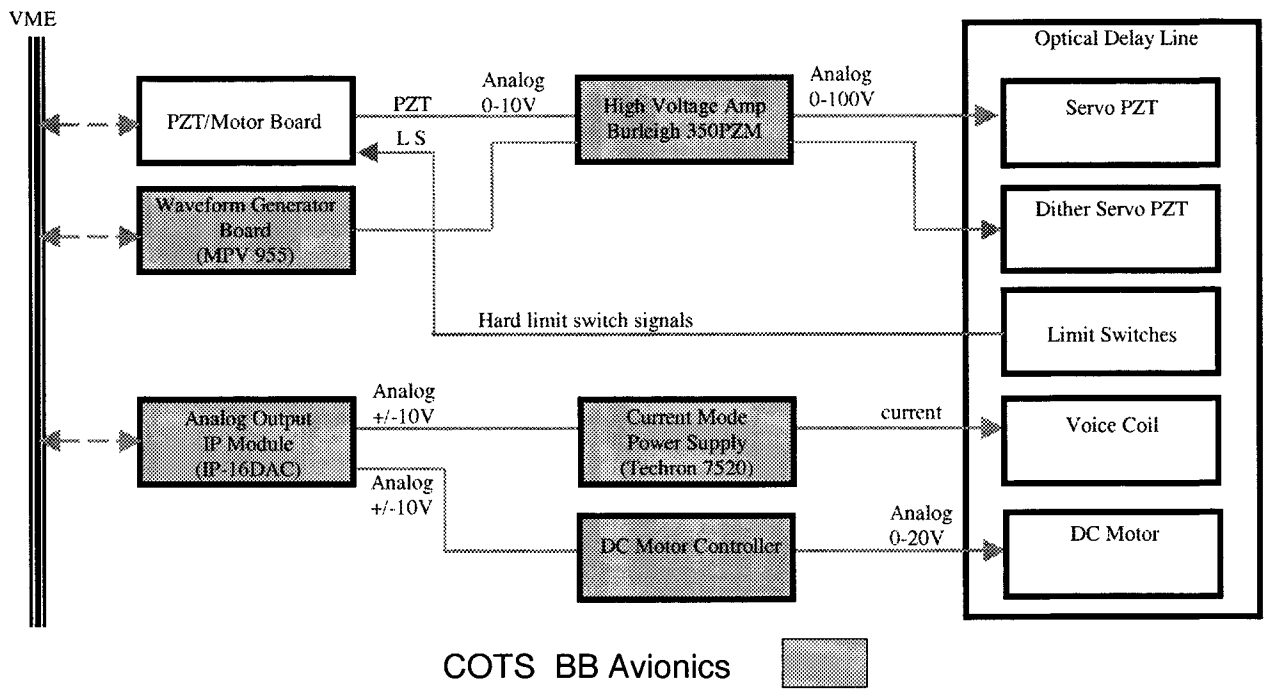

Figure 5 Optical Delay Line BB Avionics

The PZT/Motor board has analog outputs that control the servo PZT through the high voltage PZT amplifier. In addition, it provides discrete inputs for the ODL limit switches. For the flight configuration the analog output function will be handled by a space qualified IP digital analog module.

The waveform generator board is used to produce a synchronized 500Hz triangular signal for the ODL dither PZT. The signal is fed into the high voltage PZT amplifier that in turn drives the PZT. For the flight configuration a custom waveform generator circuit capable of driving the PZT is planned.

The Siderostat control BB avionics consists of the following types of components (See Figure 6):

COTS Serial Controller IP module

COTS Motor Controller

The Serial Controller IP module provides an RS232 interface to the motion controller. The siderostat can be commanded and monitored using the serial controller. For flight configuration the siderostat motors will be replaced with stepper motor type, that will be commanded by a stepper motor driver IP.

The motor controller controls 4 brushless motors with encoders. It features local control with a LCD front panel and Joy Stick or remote control using the RS232 interface. For the flight configuration the motion controller will be replaced with a space qualified stepper motor controller.

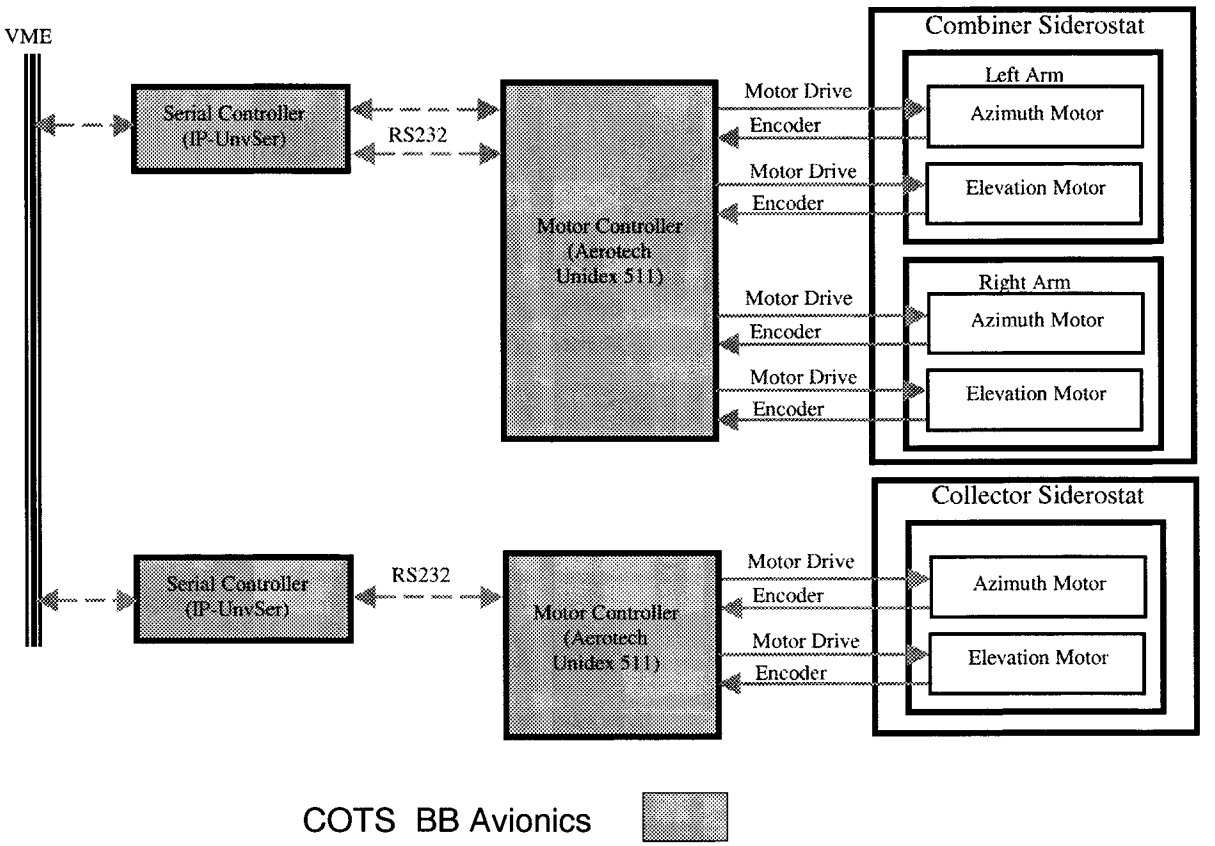

Figure 6 Siderostat BB Avionics System

The Camera interface BB avionics consists of the following types of components (See Figure 7):

Custom Camera Interface Card

The camera interface card is a JPL designed VME board that provides direct control of the CCD camera. It uses onboard RAM to store timing waveforms that are output on RS422 differential driver at a commanded rate as the card sequences through the RAM. The basic design of this card will be implemented with space-qualified board and components.

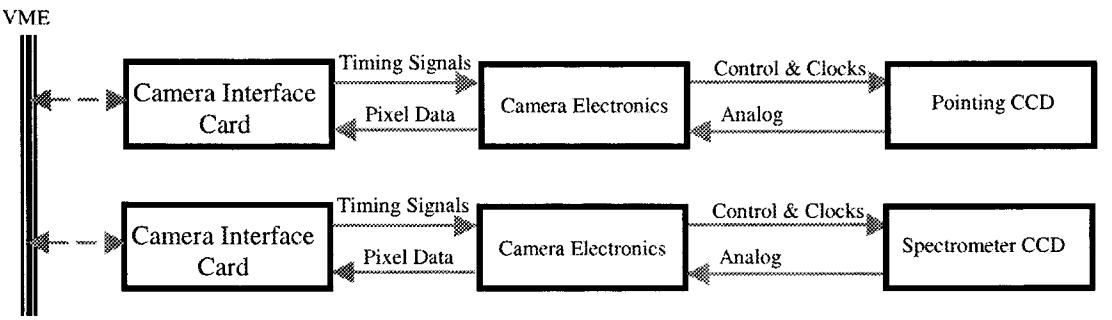

Figure 7 Siderostat BB Avionics System

The APD interface BB avionics consists of the following types of components (See Figure 8):

COTS Quadrature Decoder IP module

Custom Binning board

The quadrature decoder IP is has 4 independent quadrature counters that are configured as individual 24 bit up counters. It accepts either differential or TTL inputs. It has a maximum counting rate of 10MHz. For flight, a space-qualified version of the IP module is planned

The binning board is a custom JPL designed multiplexer board that performs the function of channeling the photon counts into each of the 4 counter inputs. This provides four photon bins that are synchronized with the control system. A flight-qualified version is planned.

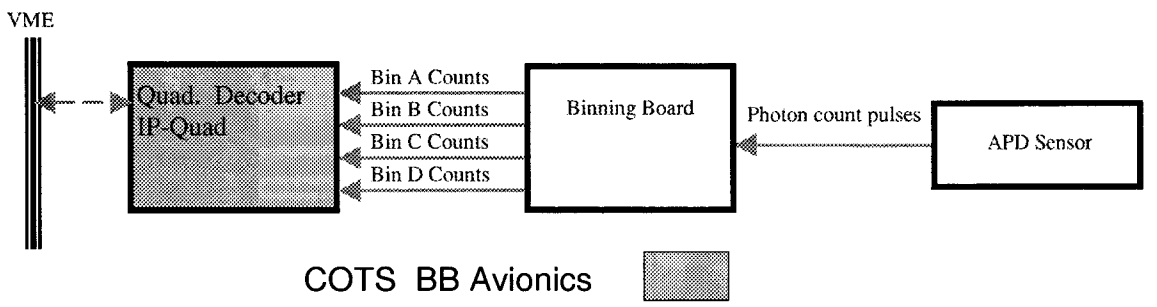

Figure 8 APD Interface BB Avionics

The Metrology interface BB avionics consists of the following types of components (See Figure 9):

Custom Phase Meter board

COTS Post Amplifier

The Phase Meter is a custom JPL designed VME card that provides 6 metrology systems. It measures the phase difference between the reference and unknown signals with very high accuracy. The existing board design will be modified to meet space flight requirements. The basic architecture and functions of the board will not be changed.

The post amplifier is a COTS device that converts the sinusoidal input signals into TTL digital outputs that can be read by the phase meters. A custom design is planned for flight.

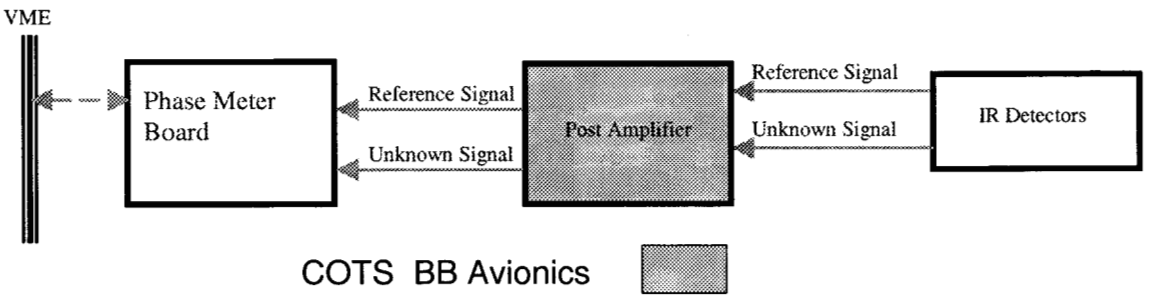

Figure 9 Metrology Interface BB Avionics System

6. CURRENT STATUS

The FIT has completed integration tests with the optical delay line and one metrology system. The preliminary version of the flight software has successfully operated on the system and has achieved closed loop control. The control system for the siderostats is currently being tested. The testbed buildup will continue as more BB components are installed.

7. SUMMARY

This paper described the application of COTS as avionics breadboards in the Formation Flying Integration Testbed that is being constructed at the Jet Propulsion Laboratory for the Space Technology 3 project. The paper highlighted the effective use of COTS as BB avionics. This technique will allow early testing of a BB avionics system which will provide sufficient lead time to incorporate changes to the flight design. The flight hardware can be based on the COTS design, which will minimize redesign of the avionics architecture, limiting changes to the flight software, and simplifing integration of the flight system.

ACKNOWLEDGEMENT

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REFERENCES

[1] John T. B. Mayer, et al, "Modern Concepts for Avionics Systems Validation Test Environments", presented at IEEE Aerospace Conference, Snowmass, CO., March 6 - 13, 1999

[2] Braden E. Hines, Richard L. Johnson, Kenneth M. Starr "Common interferometer control systems architecture," *Proceedings of the 1998 SPIE Astronomical Interferometry Conference, Kona, March 1998*

[3] Mario M. Mora "Space Interferometer Mission Testbed III (STB-3),"presented at IEEE Aerospace Conference, Snowmass, CO., March 6 - 13, 1999

[4] P. Irwin and R. Goullioud "Hardware design and object-oriented hardware driver design for the real-time interferometer control systems testbed," in *SPIE, paper 3350-76,1998*

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